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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,427	01/29/2002	Jeroen Anton Johan Leijten	NL 010073	6839
24738	7590	09/22/2005	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			RIZZUTO, KEVIN P	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/059,427

Applicant(s)

LEIJTEN, JEROEN ANTON
JOHAN

Examiner

Kevin P Rizzuto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Detailed Action

1. Acknowledgement of papers filed: Response to Non-Final Action, filed 7/1/2005.

The papers filed have been placed on record.

2. Claims 1-9 have been examined. Claims 10-15 have been cancelled, therefore, all associated objections and rejections are no longer applicable.

Priority

3. As stated in the Non-Final Office Action sent 12/2/2004, Applicant has not filed a certified copy of the European application as required by 35 U.S.C. 119(b). Therefore, Applicant's claim to foreign priority cannot be verified.

Oath/Declaration

4. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The full name of each inventor (family name and at least one given name together with any initial) has not been set forth.

5. The oath or declaration has missing letters in the inventors typed names and addresses. The scanned version of the oath on record is missing *typed* letters, the signature is not being objected to for missing letters.

Drawings

6. As stated in the Non-Final Office Action sent 12/2/2004, the drawings are objected to because figure 2 has a misspelled label "perfetech." Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Withdrawn Claim Objections and Rejections

7. Applicant, via amendment, has overcome the objections to the title and claim 4 set forth in the previous Office Action. Consequently, these objections have been withdrawn by the examiner.

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8. Applicant, via amendment, has overcome the 35 U.S.C. 102 Rejections to claims 1, 6 and 8 set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner, and new rejections are found below.

9. Applicant, via amendment, has overcome the 35 U.S.C. 103 Rejections to claims 2-5, 7 and 9 set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner, and new rejections are found below.

New Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1, 4, and 6- 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Mahin, U.S. Patent 5,819,058.

12. As per claim 1, Miller discloses a computer system with processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines

-Each memory line being fetched as a whole and being capable of holding more than one instruction: [Figure 7, multiple instructions within a memory line are shown. Also, a whole memory line is fetched, see col. 8, lines 11-29.]

-At least one instruction comprising information that signals explicitly how the processing unit, when processing the instruction from a current memory line,

should control how a part of processing is affected by crossing of a boundary to a subsequent memory line: [Compressed instructions contain a token field 112, including an end-of-packet (EP)/not-end-of-packet (NEP) field 117. The EP/NEP bit is set to indicate if the compressed instruction is at the last instruction in a packet [Col. 6, lines 20-52]. Also, compressed instructions can cross a boundary into a subsequent memory line. When an instruction packet crosses a memory boundary, the second memory must be read after in order to completely decompress the compressed instruction packet. Figs. 7 & 8, and col. 11, line 58 to col. 12, line 9].

-The processing unit being arranged to respond to the information by controlling said part as signaled by the information: [Figs. 7 & 8, and col. 11, line 58 to col. 12, line 9 describe the action taking to handle the boundary crossing].

-The information is inserted to the instructions at compile time: Col. 6, lines 53-58]

13. As per claim 4, Miller teaches wherein information signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information (Column 11, lines 35-45, Column 12, lines 10-25 and figures 7 and 8; Miller teaches that the addressing system determines that a next instruction packet has a pad instruction in front of it. It is inherent that there is

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information that explicitly signals the addressing system in order for the addressing system to determine there is a pad instruction, a determination couldn't be made by hardware without an explicit signal. The pad instruction is then discarded and does not cause any operation to occur in the processor, and the Aright and Aleft addresses (program counters) are incremented to point to a new memory line, therefore the pad instruction is skipped over. The Aright address points to byte 12 in memory 282 (a subsequent memory line) and Aleft points to byte 16 (a subsequent memory line) of memory 280.)

14. As per claim 6, a computer system according to claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to the functional units: [Figs. 5, 6 and 9. Col. 2, lines 27-63]

-The instructions being VLIW instructions, capable of containing two or more operations: [Figs. 5, 6 and 9. Col. 2, lines 27-63]

-The instruction comprising a field distinct from the operations to specify said information: [Fig. 4, Token field 134, col. 5, lines 39-53.]

15. As per claim 7, Miller teaches a computer system according to claim 6, the field comprising, in addition to said information, a decompression code that specifies for which issue slots the instruction contains operations: [Col. 5, lines 39-53, figs. 5 & 6. The token indicates the instruction type and "identifies the processing unit."]

16. As per claim 8, given the similarities between claim 1 and claim 8, the arguments as stated for the rejection of claim 1 also apply to claim 8.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 5,819,058, in view of Mohamed, U.S. Patent 6,684,319.

19. As per claim 2, Miller fails to teach selectively loading prefetched instructions based on the information in the token field.

20. Mohamed teaches wherein information signals explicitly whether or not the subsequent memory line has to be prefetched during processing of VLIW instructions, the processing unit being arranged to start prefetching of the subsequent memory line in response to the information: (Column 3, lines 35-60)

21. It would have been obvious to combine the prefetch instruction flag bit of Mohamed with the processor of Miller because of the advantages explained in Mohamed in col. 2, lines 35-64, including decreasing the power consumed that is normally associated with prefetching and the time required when fetching long instructions. The prefetching of long instruction words (128 or 256 bits for example) can cause a significant amount of power to be consumed (column 1, lines 21-32 of Mohamed). Therefore, adding an additional bit for selective prefetching as taught by Mohamed would have saved power, because not every line would need to be

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prefetched, only those that are necessary. This advantage of using less power would have provided the motivation to add the prefetch instruction flag bit.

22. As per claim 3, a computer system according to Claim 2, wherein the information contains a prefetch bit whose value signals explicitly whether or not the subsequent memory line has to be prefetched: (The combination of Miller and Mohamed as applied to claim 2 teaches the limitations of claim 3. See column 3, lines 35-60 of Mohamed)

23. As per claim 9, given the similarities between claim 2 and claim 9, the arguments as stated for the rejection of claim 2 also apply to claim 9. Examiner notes that the claim language requires "at least one of" a list of things, therefore this combination of Miller and Mohamed is sufficient to reject claim 9.

24. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 5,819,058, as applied to claim 1, in view of Keller, U.S. Patent 6,546,478.

25. As per claims 5, Miller failed to teach wherein the information signals explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

26. Keller teaches information that signals (Continuation field 126 of figure 8) explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being

arranged to stall in response to the information when the instruction is reached from the branching instruction: (Column 22, lines 1-17, column 23, lines 17-24 and column 26, line 44 to column 27, line 8; The invention of Keller uses the same PC address used to fetch instructions from the I-cache to fetch a line predictor entry 82 of figure 6 (PC shown in fig. 3). This entry contains information, including the continuation bit 126 (figure 8), which is combined with the instruction to be decoded by the decoder (fig. 4, fig. 22).

27. This information, while associated with the instruction and addressed by the same address as the instruction, is stored in a different memory than the instruction. It would also have been obvious to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since it has been held that the use of a one piece construction (instead of the two piece line predictor entry structure and I-cache disclosed in Keller) "would be merely a matter of obvious engineering choice." *In re Larson*, 340 F.2d 965,968, 144 USPQ 347,349 (CCPA 1965).

28. Adding the continuation bit to the instruction information bits that already exist would allow the processor to know whether a branch target instruction crosses a boundary in the cache and a stall should occur to fetch the next cache line. The processor could detect the need for a memory access quickly and easily if the continuation bit was included in the cache line. The earlier a memory access is known to be needed the better, because it is well known in the art that memory accesses can be costly to processing speed. Specifically in this application, the earlier the memory access is known, the earlier the instruction is fetched from memory and the earlier the

instruction can be decompressed and dispatched. It would have been obvious to combine the continuation bit within the cache line of Miller because of the advantages provided above.

Response to Arguments

29. Applicants arguments filed on 7/1/2005 have been fully considered but they are moot in view of the new rejections above.

Conclusion

1. **THIS ACTION IS MADE FINAL.** The amendments to the claims have caused the need for the new rejections. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

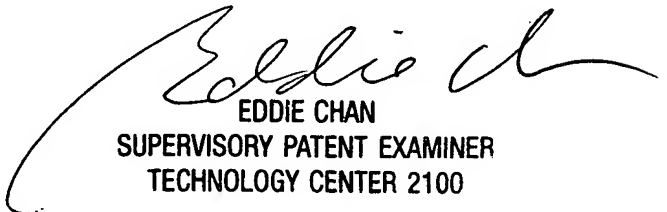
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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR


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